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10/616,302

07/10/2003

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07/12/2004

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EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|--------------------------------------|--|
| Office Action Summary | Application No. 10/616,302 | Applicant(s) LIM ET AL. <i>OK</i> | |
| | Examiner Paul E Brock II | Art Unit 2815 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 1-5 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 6-10 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group II, claims 6 – 10 in the reply filed on May 17, 2004 is acknowledged. The traversal is on the ground(s) that the product defined in claims 1 – 5 is manufactured by the process of claims 6 – 10, and thus, claims 1 – 10 define a single inventive concept. This is not found persuasive because as stated in the restriction requirement dated April 20, 2004, the device may be made by selective deposition, which is different than the method claimed.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 1 – 5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on May 17, 2004.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: While claim 7 recites “supplying a RF power of about 700° C” the specification only provides support for “[a] RF power is below about 700° C”.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6 – 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 6, it is not clear if two semiconductor layers are being defined in the claim recitations “forming a semiconductor layer including at least a gate insulation layer; forming a silicon layer on the gate insulation layer.” Are there two semiconductor layers, the “a semiconductor layer” and the “a silicon layer”? For purposes of this office action “forming a semiconductor layer including at least a gate insulation layer;” will be considered -- forming a layer including at least a gate insulation layer; --.

With regard to claim 7, it is not clear what layer is being formed by the limitation “wherein at the step of forming the reaction prevention layer, the silicon layer is formed by performing a ... nitridation”. Is the reaction prevention layer formed by a nitridation, or is the silicon layer formed by a nitridation? For purposes of this office action “wherein at the step of forming the reaction prevention layer, the silicon layer is formed by” will be considered -- wherein at the step of forming the reaction prevention layer, the reaction prevention layer is formed by --.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 6, and 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (USAPT 4935804, Ito) in view of applicant's admitted prior art (AAPA).

With regard to claim 6, Ito discloses in figures 1 – 4 a method for fabricating a semiconductor device. Ito discloses in figure 1 forming a layer including at least a gate insulation layer (3). Ito discloses in figure 2 forming a silicon layer (4) on the gate insulation layer. Ito discloses in figure 2 and column 2, lines 43 – 55 forming a reaction prevention layer (5) on the silicon layer, the reaction prevention layer containing nitrogen and silicon. Ito discloses in column 2, lines 43 – 47 wherein the reaction prevention layer has a thickness of 2 nm (i.e. 20 angstroms is equivalent to 2 nm). One of ordinary skill in the art would recognize that the thickness of a reaction prevention layer of silicon nitride, as disclosed by Ito, is directly proportional to the surface density of nitrogen. Further, a reaction prevention layer of silicon nitride having a thickness of 2nm would inherently have a surface density of nitrogen above about $1 \times 10^{15} / \text{cm}^2$. Ito discloses in figure 3 forming a metal layer (6) on the reaction prevention layer. Ito discloses in figure 3 forming a stack gate electrode by etching sequentially the metal layer, the reaction prevention layer and the silicon layer. Ito teaches forming a PSG film (9) on the sidewalls of the silicon layer. Ito does not teach performing a

Art Unit: 2815

selective oxidation process oxidizing selectively the silicon layer from the stack gate electrode.

AAPA teaches on page 1, line 25 – page 2, line 10 performing a selective oxidation process oxidizing selectively the silicon layer from the stack gate electrode. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the selective oxidation process of the AAPA in the method of Ito in order to recover a damaged gate oxide layer which resulted from the gate stack etch and therefore increase the reliability of the device as stated by the AAPA on page 1, line 25 – page 2, line 10.

With regard to claim 8, Ito discloses in column 2, lines 43 – 47 wherein at the step of forming the reaction prevention layer, a surface of the silicon layer is proceeded with a thermal treatment performed at a temperature ranging from about 750° C to about 950° C. for about 10 seconds to about 100 seconds in an atmosphere of NH₃ (ammonia). It should be noted that about 750° C to about 950° C is obvious in view of the disclosure of 700° C as taught by Ito. (See MPEP2144.05 II).

With regard to claim 9, Ito discloses in figure 2 and column 2, lines 48 – 51 wherein the reaction prevention layer is a silicon nitride layer formed through the use of a chemical vapor deposition technique or an atomic layer deposition technique.

With regard to claim 10, Ito discloses in figure 2 and column 2, lines 48 – 51 wherein the reaction prevention layer is formed with a thickness of 1 – 5 nm (10 Å is equivalent to 1 nm). It should be noted that thicker than about 1.2 nm but thinner than about 3 nm is obvious in view of Ito's disclosure of 1 – 5 nm. (See MPEP 2144.05 I).

Art Unit: 2815

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito and the AAPA as applied to claim 6 above, and further in view of Chen et al. (USPAT 6727134, Chen).

With regard to claim 7, Ito discloses in column 2, lines 48 – 51 wherein at the step of forming the reaction prevention layer, the reaction prevention layer is formed by performing a nitridation process using an ammonia based plasma deposition technique to form a silicon nitride layer. It is not clear what plasma deposition technique Ito uses. Chen teaches in figure 1 and column 2, line 55 – column 3, line 12 wherein at the step of forming a silicon nitride layer, the silicon nitride layer is formed by performing a remote plasma nitridation (RPN) technique in an atmosphere of NH_3 as simultaneously as by maintaining a substrate temperature in a range from about 0°C to about 700°C and supplying a RF power of about 300 W. It should be noted that it is further obvious to have an RF power of about 1000 W in view of the teaching of 100 – 300 W in Chen. (See MPEP 2144.05 II). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the RPN technique of Chen in the method of Ito and the AAPA in order to use an ammonia based plasma deposition that is well understood in the art.

Conclusion

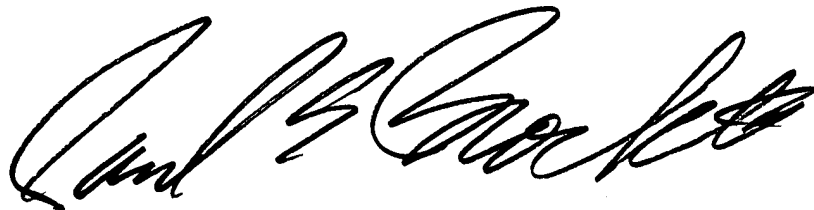
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Minazu, Suehiro et al. '410, and Suehiro et al. '193 all teach forming a nitride layer on a silicon gate electrode layer. The Suehiro references also teach a relationship between a silicon nitride layer thickness and a surface density of nitrogen.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II

A handwritten signature in black ink, appearing to read 'Paul E Brock II', with a stylized, cursive script.